UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,327	12/09/2004	Roland Brandl	AT02 0034 US	2949

65913 7590 09/27/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
09/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/517,327	BRANDL, ROLAND	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

The applicant is advised that a certified English translation of the applicant's foreign priority document EPO 02100694.5 is required in order to claim full benefit of the foreign priority date.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

`Arrangement of the Specification`

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Rao et al., Patent No. 5,770,886.

With respect to claim 1, applicant's acknowledged prior art [Fig. 1] teaches a data carrier [Fig. 1, 1] that includes an integrated circuit [Fig. 1, 5] which comprises a first terminal and a second terminal [Fig. 1, 6, 7], wherein the two terminals are provided for connection with transmission means [Fig. 1, 2] of the data carrier and an ESD protection circuit [Fig. 1, 8], which is connected between the two terminals [Fig. 1, 6, 7] and which comprises a series connection [Fig. 1, 9] consisting of a first protection diode [Fig. 1, 10] and a protection stage [Fig. 1, 11], which protection stage may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and a rectifier circuit [Fig. 1, 13], which is connected to the ESD protection circuit [Fig. 1, 8] and comprises a rectifier diode [Fig. 1, 14] connected in parallel with the ESD protection circuit as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig. 1.

However, the prior art fails to teach or suggest that a rectifier diode of the rectifier circuit takes the form of a Schottky diode with a parasitic p/n junction and wherein the Schottky diode with the parasitic p/n junction forms a second protection diode of the ESD protection circuit.

Rao discloses an ESD protection circuit. Rao discloses an ESD protection circuit [Fig. 6, 101] and a rectifier diode [Fig. 6; 11], which takes the form of a Schottky diode with a parasitic p/n junction [Fig. 6; the Schottky diode 11 inherently has a parasitic pn junction; as shown per applicant's own Fig. 3] forms the second protection diode of the ESD protection circuit [Fig. 6; Schottky diode turns on when there is excessive amount of current flowing in the reverse direction, and protects the circuit elements] connected between a power supply [Fig. 6, 15] and a ground [Fig. 6; col. 8; lines 8-12].

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Rao's Schottky diode which is in parallel with ESD protection circuit as a second protection diode of the ESD protection circuit, with the integrated circuit for a data carrier of the applicant's acknowledged prior art because any abnormal reverse voltage applied to the LED system turns on the Schottky diode and diverts a large portion of any abnormal reverse current away via the Schottky diode. Schottky diodes are well known for their ability to handle large reverse currents with negative effects.

With respect to claim 2, the acknowledged prior art teaches that the rectifier circuit [Fig. 1, 13] takes the form of a voltage doubler circuit [Specifications, Page 4, line 34].

With respect to claim 3, applicant's acknowledged prior art [Fig. 1] teaches a data carrier [Fig. 1, 1] for contactless communication with a communications stations, which data carrier comprises transmission means [Fig. 1, 2, Specification, Page 4, lines 1-6] and an integrated circuit [Fig. 1, 5] connected with the transmission means, which

integrated circuit comprises a first terminal and a second terminal [Fig. 1, 6, 7], wherein the two terminals are provided for connection with transmission means [Fig. 1, 2] of the data carrier and an ESD protection circuit [Fig. 1, 8], which is connected between the two terminals [Fig. 1, 6, 7] and which comprises a series connection [Fig. 1, 9] consisting of a first protection diode [Fig. 1, 10] and a protection stage [Fig. 1, 11], which protection stage may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and a rectifier circuit [Fig. 1, 13], which is connected to the ESD protection circuit [Fig. 1, 8] and comprises a rectifier diode [Fig. 1, 14] connected in parallel with the ESD protection circuit as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig. 1. Claim 3 differs from claim 1 by having a data carrier for contactless communication with a communications station. The teachings of Rao would apply to reject claim 3.

With respect to claim 4, the acknowledged prior art [Fig. 1] teaches that the rectifier circuit [Fig. 1, 13] takes the form of a voltage doubler circuit [Specifications, Page 4, line 34].

With respect to claim 5, applicant's acknowledged prior art [Fig. 1] teaches an integrated circuit [Fig. 1, 5] comprising an ESD protection circuit [Fig. 1, 8] coupled between a first node [Fig. 1, 6] and a second node [Fig. 1, 7], the ESD protection circuit having a first diode [Fig. 1, 10] coupled anode-to-cathode between the first node and the second node; and a rectifier circuit [Fig. 1, 13] coupled between the first node [Fig. 1, 6] and the second node [Fig. 1, 7]. However, the acknowledged prior art does not disclose a rectifier circuit having a Schottky diode, the Schottky diode comprising a

parasitic p/n junction diode coupled anode-to-cathode between the second node and the first node.

Rao discloses an ESD protection circuit. Rao discloses an ESD protection circuit [Fig. 6, 101; col. 8; lines 8-12] and a rectifier diode [Fig. 6; 11; Schottky diode turns on when there is excessive amount of current flowing in the reverse direction, and protects the circuit elements]], which takes the form of a Schottky diode comprising a parasitic p/n junction [Fig. 6; the Schottky diode 11 inherently has a parasitic pn junction; as shown per applicant's own Fig. 3] coupled anode [Fig. 6; 17] to cathode [Fig. 6; 14] between the second node [Fig. 6; GND] and the first node [Fig. 6; IN 15]; wherein the parasitic pn junction diode provide a second protection diode.

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Rao's Schottky diode which is in parallel with ESD protection circuit as a second protection diode of the ESD protection circuit, with the integrated circuit for a data carrier of the applicant's acknowledged prior art because any abnormal reverse voltage applied to the LED system turns on the Schottky diode and diverts a large portion of any abnormal reverse current away via the Schottky diode. Schottky diodes are well known for their ability to handle large reverse currents with negative effects.

With respect to claim 6, the acknowledged prior art teaches that the first node [Fig. 1, 6] and the second node [Fig. 1, 7] are connected to a dipole antenna [Fig. 1, 3].

Response to Arguments

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dharti H. Patel/
GAU 2836
09/17/2007

9/17/07

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800